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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,091	08/28/2001	Tae-sung Jung	5649-886	5816

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EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,091	JUNG ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-25,27-29,31-35 and 37-44* is/are rejected.

7)☒ Claim(s) *5,6,26,30 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/28/01,12/23/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-44 are presented for examination.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.

Drawings

4. Figure 6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 2, 8-13, 16-23 and 43-44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitations "the delay time" in line 8, "the output signal" in line 9. There are insufficient antecedent basis for those limitations in the claim.

Claim 2 is rejected because they incorporate the deficiencies of claim 1.

Claim 8 recites the limitation "the output signal" in lines 9-10. There is insufficient antecedent basis for those limitations in the claim.

Claims 9-13 are rejected because they incorporate the deficiencies of claim 8.

Claim 16 recites the limitations "the delay time" in line 1, "the output signal" in line 1. There are insufficient antecedent basis for those limitations in the claim.

Claims 17-19 are rejected because they incorporate the deficiencies of claim 16.

Claim 20 recites the limitations "the delay time" in line 1, "the clock signal" in line 8. There are insufficient antecedent basis for those limitations in the claim.

Claims 21-23 are rejected because they incorporate the deficiencies of claim 20.

Claim 43 recites the limitation "the memory device" in line 5. There is insufficient antecedent basis for those limitations in the claim.

Claim 44 is rejected because they incorporate the deficiencies of claim 43.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-4, 7-10, 12-18, 20-22, 24, 25, 27-29, 31-35 and 37-44 are rejected under 35 U.S.C. 102(e) as being anticipated by McClannahan (McClannahan), U.S. patent no. 6,438,670.

As per claim 1, McClannahan discloses that a semiconductor memory device controlled by a memory controller [fig. 5], comprising:

a delay control register [26, fig. 1] for receiving delay control information from the memory controller [memory controller 10] and storing the received delay control information [fig. 1; col.6, lines 8-13; col. 8, lines 49-51]; and

an input buffer for receiving a command signal, an address signal, and write data from the memory controller and delaying the received command signal, address signal, and write data [fig. 6; col. 8, lines 53-63];

wherein a delay time of the input buffer is controlled in response to an output signal of the delay control register [col. 5, lines 50-52, 61-63; col. 6, lines 19-29; figures 10, 11].

As per claim 2, McClannahan discloses that the input buffer comprises: a delay controller for setting a predetermined delay time in response to the output signal of the delay control register; a data input buffer for delaying the write data in response to the output signal of the delay controller; an address input buffer of delaying the address

signal in response to the output signal of the delay controller; and a command input buffer for delaying the command signal in response to the output signal of the delay controller [figures. 5-7; col. 5, lines 50-52, 61-63; col. 6, lines 19-29; col. 8, lines 53-63].

As per claim 3, McClannahan discloses that a memory controller for controlling memory modules [74, 74a, fig. 5], into which a plurality of semiconductor memory devices [76, fig. 5] are loaded, comprising:

a module selector [84, fig. 6] for outputting a module selection signal for selecting the memory modules in response to a clock signal [col. 9, lines 18-23];

a delay control register for receiving delay control information according to a specification from serial presence detectors (SPD) loaded into the memory modules [col. 8, lines 42-51] and storing the received delay control information [fig. 1; col.6, lines 8-13; col. 8, lines 49-51]; and

an output buffer for delaying an internal command signal, an internal address signal, and write data in response to the output signal of the module selector and outputting the delayed write data to the semiconductor memory device [fig. 6; col. 8, lines 53-66];

wherein the delay time of the output buffer is controlled in response to the output signal of the delay control register [col. 5, lines 50-52, 61-63; col. 6, lines 19-29; figures 10, 11].

As per claim 4, McClannahan discloses the memory controller further comprises an input buffer, whose delay time is controlled in response to the output signal of the delay control register, the input buffer for delaying read data received from the

semiconductor memory device and outputting the delayed read data to the inside of the memory controller [fig. 6; col. 8, lines 53-66].

As per claim 7, McClannahan discloses that the input buffer comprises: a delay controller for setting a predetermined delay time in response to an output signal of the delay control register [col.6, lines 8-13; col. 8, lines 49-51]; and a data input buffer for delaying read data received from the semiconductor memory device and outputting the delayed read data to the inside thereof in response to the output signal of the delay controller [figures 6, 7; col. 8, lines 53-66].

As per claim 8, McClannahan discloses that a memory system [fig. 5] comprising memory modules, into which a plurality of semiconductor memory devices are loaded, and a memory controller [78, figures 5, 6] for controlling the memory modules,

wherein the memory modules comprises SPDs for storing predetermined control information [timing parameter] according to the specification of the memory module [col. 8, lines 42-51], and

wherein the memory controller comprises: a delay control register for receiving the predetermined delay information from the SPDs and storing the received delay control information [fig. 1; col.6, lines 8-13; col. 8, lines 49-51]; and

an output buffer, whose delay time is controlled in response to the output signal of the delay control register, the output buffer for delaying a command signal, an address signal, and write data, and outputting the delayed command signal, address signal, and write data to the semiconductor memory device [fig. 6; col. 8, lines 53-66].

As per claim 9, McClannahan discloses the memory controller further comprises an input buffer, whose delay time is controlled in response to the output signal of the delay control register, the input buffer for delaying read data received from the semiconductor memory device and outputting to the inside of the memory controller. [fig. 6; col. 8, lines 53-66].

As per claim 10, McClannahan discloses that the input buffer comprises: a delay controller for setting a predetermined delay time in response to an enable signal and the output signal of the delay control register [col.6, lines 8-13; col. 8, lines 49-51]; and a data input buffer for delaying read data received from the semiconductor memory device and outputting the delayed read data to the inside thereof in response to the output signal of the delay controller [figures 6, 7; col. 8, lines 53-66].

As per claim 12, McClannahan discloses that each of the semiconductor memory devices comprises:

a delay control register for receiving delay control information from the memory controller and storing the received delay control information [fig. 1; col.6, lines 8-13; col. 8, lines 49-51]; and

an input buffer for receiving a command signal, an address signal, and write data from the memory controller and delaying the received command signal, address signal, and write data [fig. 6; col. 8, lines 53-63];

wherein the delay time of the input buffer is controlled in response to the output signal of the delay control register [col. 5, lines 50-52, 61-63; col. 6, lines 19-29; figures 10, 11].

As per claim 13, McClannahan discloses that the input buffer comprises: a delay controller for setting a predetermined delay time in response to the output signal of the delay control register; a data input buffer for delaying the write data in response to the output signal of the delay controller; an address input buffer of delaying the address signal in response to the output signal of the delay controller; and a command input buffer for delaying the command signal in response to the output signal of the delay controller [figures. 5-7; col. 5, lines 50-52, 61-63; col. 6, lines 19-29; col. 8, lines 53-63].

As to claims 14-18 and 20-22, McClannahan basically teaches the corresponding elements as set forth in claims 1-13 that are carried out the method of operating steps in claims 14-18. McClannahan teaches the claimed system. Therefore, McClannahan teaches the claimed method of steps to carry out the system.

As per claim 24 is contained the same limitations as set forth claim 8. Therefore, same rejection is applied.

As per claim 25, McClannahan discloses that the memory controller further comprises: a delay control register that is configured to receive and to store the delay control information therein [fig. 1; col.6, lines 8-13; col. 8, lines 49-51]; and

an output buffer that is configured to generate the control signal in response to an input control signal and the delay control information stored in the delay control register [fig. 6; col. 8, lines 53-66].

As per claim 27, McClannahan discloses that the memory controller further comprises: an input buffer that is configured to receive data from the respective one of the plurality of memory modules at an input thereof and to provide the received data at

an output thereof in response to the delay control information stored in the delay control register [fig. 6; col. 8, lines 42-66].

As per claim 28, McClannahan discloses that the control signal comprises a command control signal, an address control signal, and data, and wherein the output buffer comprises a command output buffer that is configured to generate the command control signal in response to an input command control signal and the delay control information stored in the delay control register, an address output buffer that is configured to generate the address control signal in response to an input address control signal and the delay information stored in the delay control register, and a data output buffer that is configured to generate the data in response to input data and the delay information stored in the delay control register [figures. 5-7; col. 5, lines 50-52, 61-63; col. 6, lines 19-29; col. 8, lines 53-63].

As per claim 29, McClannahan discloses that at least one of the plurality of memory modules comprises a plurality of memory devices [fig. 5; col. 8, lines 13-18].

As per claim 31 is contained the same limitations as set forth claim 1. Therefore, same rejection is applied.

As to claims 32-33 are contained the same limitations as set forth claims 27-28 respectively. Therefore, same rejection is applied.

As per claim 34 is contained the same limitations as set forth claim 8. Therefore, same rejection is applied.

As per claims 35 and 37 are contained the same limitations as set forth claim 27-28 respectively. Therefore, same rejection is applied.

As to claims 38-44, McClannahan basically teaches the corresponding elements that are carried out the method of operating steps. McClannahan teaches the claimed system. Therefore, McClannahan teaches the claimed method of steps to carry out the system.

Allowable Subject Matter

9. Claims 5, 6, 11, 19, 23, 26, 30, 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chun Cao

Oct. 27, 2004